Consequently, when no error-containing code is detected from one sector by syndrome calculation, the subsequent error correcting process becomes unnecessary, which can greatly reduce the time required for error correction. Above all, recent improvements in manufacturing techniques and materials of CD-ROMs reduces the occurrence of minor blemishes due to manufacturing errors or inappropriate handling of users, so that few code words are subjected to error correction. As a result, the subsequent code words do not need to be processed in most cases, thereby increasing the effects of the present invention.

The aspect 4 provides the aspect 3 with the same actions and effects as those which the aspect 2 provides for the aspect 1.

The aspect 5 relates to an error correction device comprising: a buffer memory for storing at least one sector of data having a structure where each of N words of error correcting code comprises a data unit, an inner code parity unit, and one error detecting code; a syndrome calculating means for generating syndrome for data read from the buffer memory; an error correcting means for correcting error-containing data in the buffer memory by detecting an error position from the syndrome generated by the syndrome calculating means and by calculating an error value; an error detecting means for detecting an error, one sector at a time, in error-corrected data generated by the error correcting means; a storing means for storing mid-term results, in code word units, of an error detecting process in the error detecting means; a bus control means for controlling data transfer between the buffer memory, the syndrome calculating means, the error correcting means, and the error detecting

means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times.

The bus control means executes a first transfer where data to be corrected are transferred in code word units from the buffer memory concurrently to the syndrome calculating means and to the error detecting means until the syndrome calculating means detects an error-containing code. The bus control means suspends the first transfer when the syndrome calculating means has detected an error-containing code, and executes a second transfer where the error-corrected code word is transferred from the buffer memory to the error detecting means after the error correction done by the error correcting means for the code word including an error-containing code. After the completion of the second transfer, the first transfer for subsequent code words is resumed. This process is executed every time an error-containing code is detected.

The error detecting means, until the syndrome calculating means detects an error-containing code, executes a first error detection where error detection is performed for a code word transmitted from the buffer memory in parallel with the syndrome calculation done by the syndrome calculating means, while storing mid-term results of the error detection in code word units to the storing means. After the syndrome calculating means detects an error-containing code, the error detecting means executes error detection for code words whose errors have been detected and corrected by the error correcting means, and stores them in the next position in the storing means. After the completion of the error detection for the code words, the first error detection is resumed. These processes

are repeated every time the syndrome calculating means detects an error-containing code.

Thus, by exclusively re-transferring the data of the code word from which an error-containing code is detected and corrected to the error detector, the sequential process of error-containing code detection, error correction, and error detection can be executed in parallel, thereby greatly reducing the time required for error correction.

The aspect 6 provides the aspect 5 with the same actions and effects as those which the aspect 2 provides for the aspect 1.

The aspect 7 relates to an error correction device comprising; a buffer memory for storing at least one ECC block of data (one ECC block is enough in the present aspect) having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction, for example, sector as a unit, are subjected to error correction a syndrome calculating means for generating syndrome for data read from the buffer memory; an error correcting means for correcting error-containing data in the buffer memory by detecting an error position from the syndrome generated by the syndrome calculating means and by calculating an error value; an error detecting means for detecting an error in error-corrected data generated by the error correcting means; a bus control means for controlling data transfer between the buffer memory, the syndrome calculating means, the error correcting means, and the error